Komponenten zum Zählen und zur Messung von Zeitparametern

Zähler und Zeitgeber

Aufgaben:

1. zählen
2. messen
3. erzeugen
4. überwachen

1.) Ereignisse zählen

2.) Zeiten messen
Frequenzen messen
Perioden messen
Tastverhältnisse messen (PWM-Signale dekodieren)

3.) Zeitintervalle erzeugen
Impulsfolgen erzeugen
Frequenzen erzeugen
PWM-Signale erzeugen

4.) Ausbleibende Ereignisse detektieren
Zeitstempel erzeugen

Watchdog-Timer: Maßnahme zur Erkennung von Fehlern.

Programmierbare Zähler/ Zeitgeber

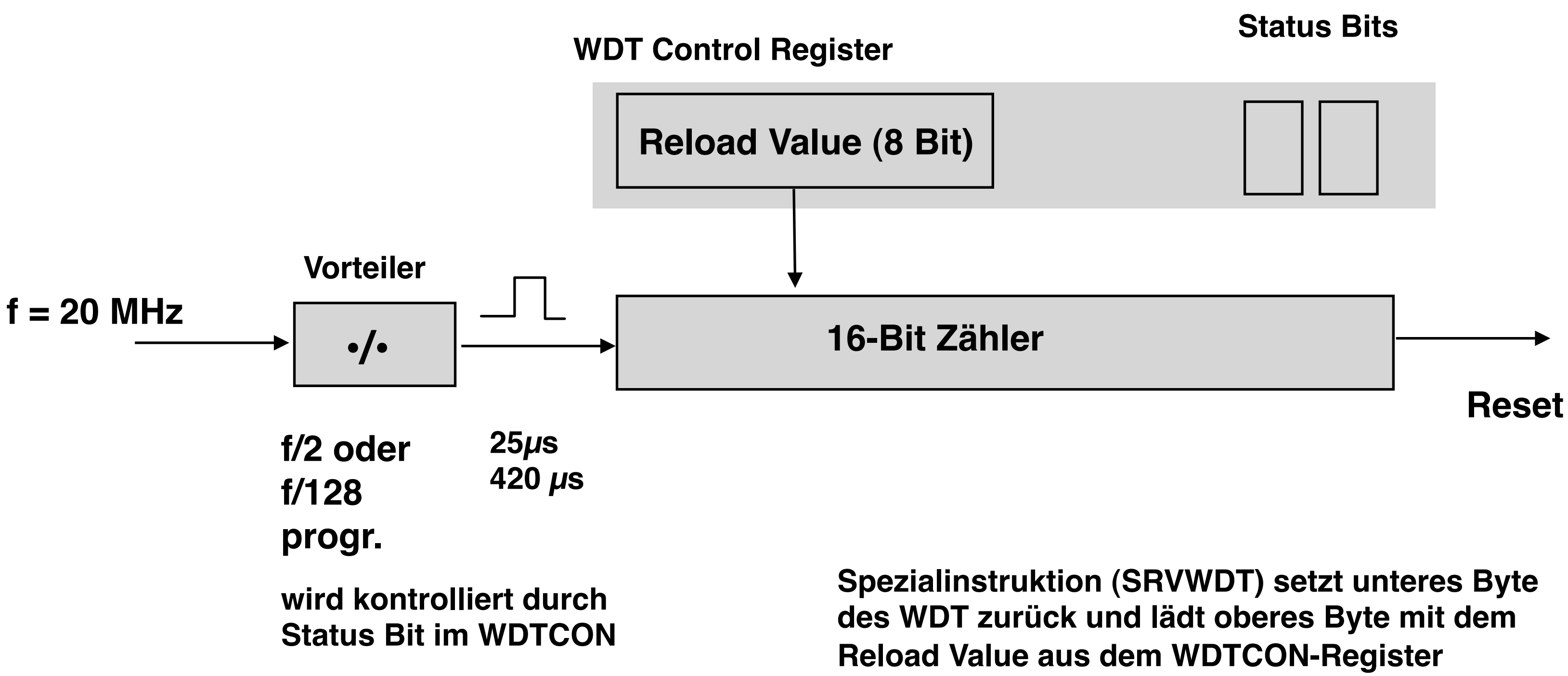
- allgemeine Fuktionen
- Capture & Compare
- Puls-Weiten-Modulation (PWM)

Fallbeispiele:

Hitachi H8/300
AVR

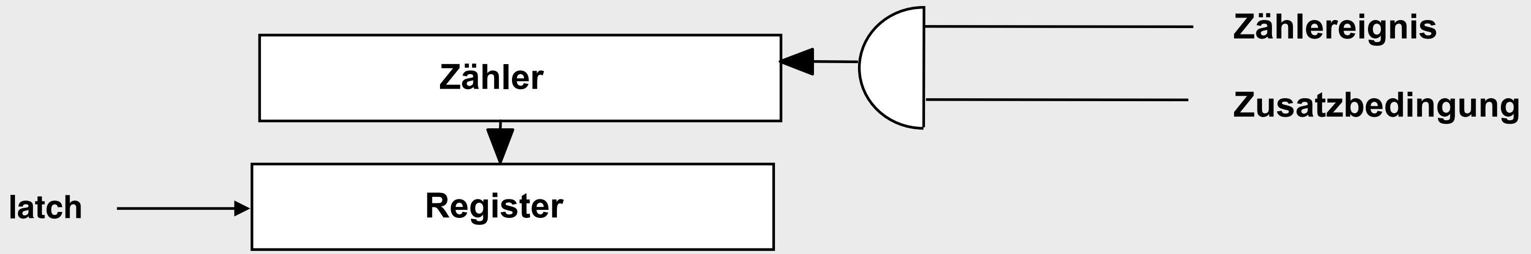
C167 Watchdog Timer

Der Watchdog-Timer wird bei der Initialisierung des Micro-Controllers aktiviert und läuft danach ununterbrochen. Wird er nicht rechtzeitig zurückgesetzt, löst er einen Reset und damit Neustart der Systemsoftware aus. Ein WDT kann durch Software nach der Initialisierung nicht deaktiviert werden.

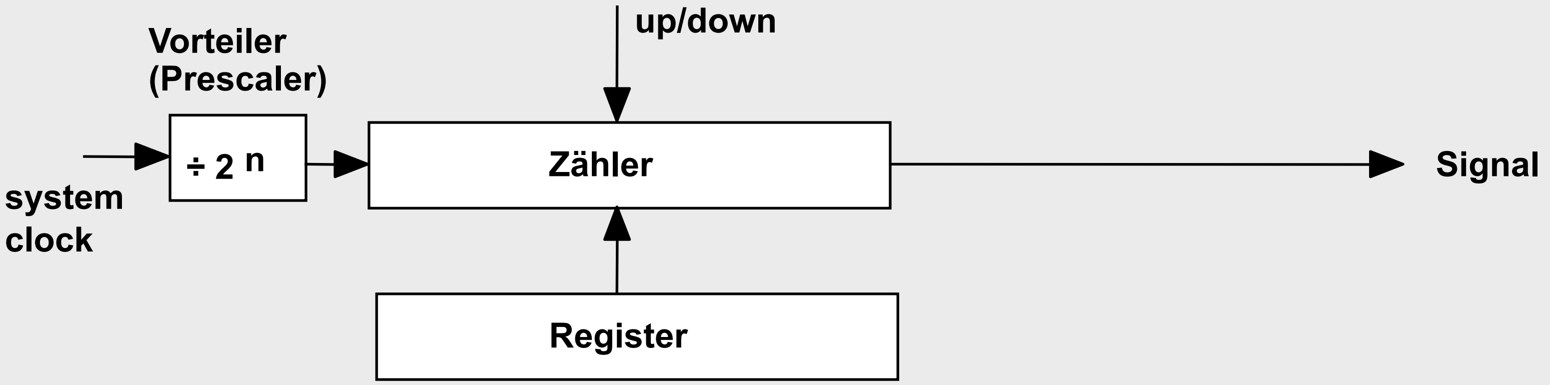


Allgemeine Funktionen

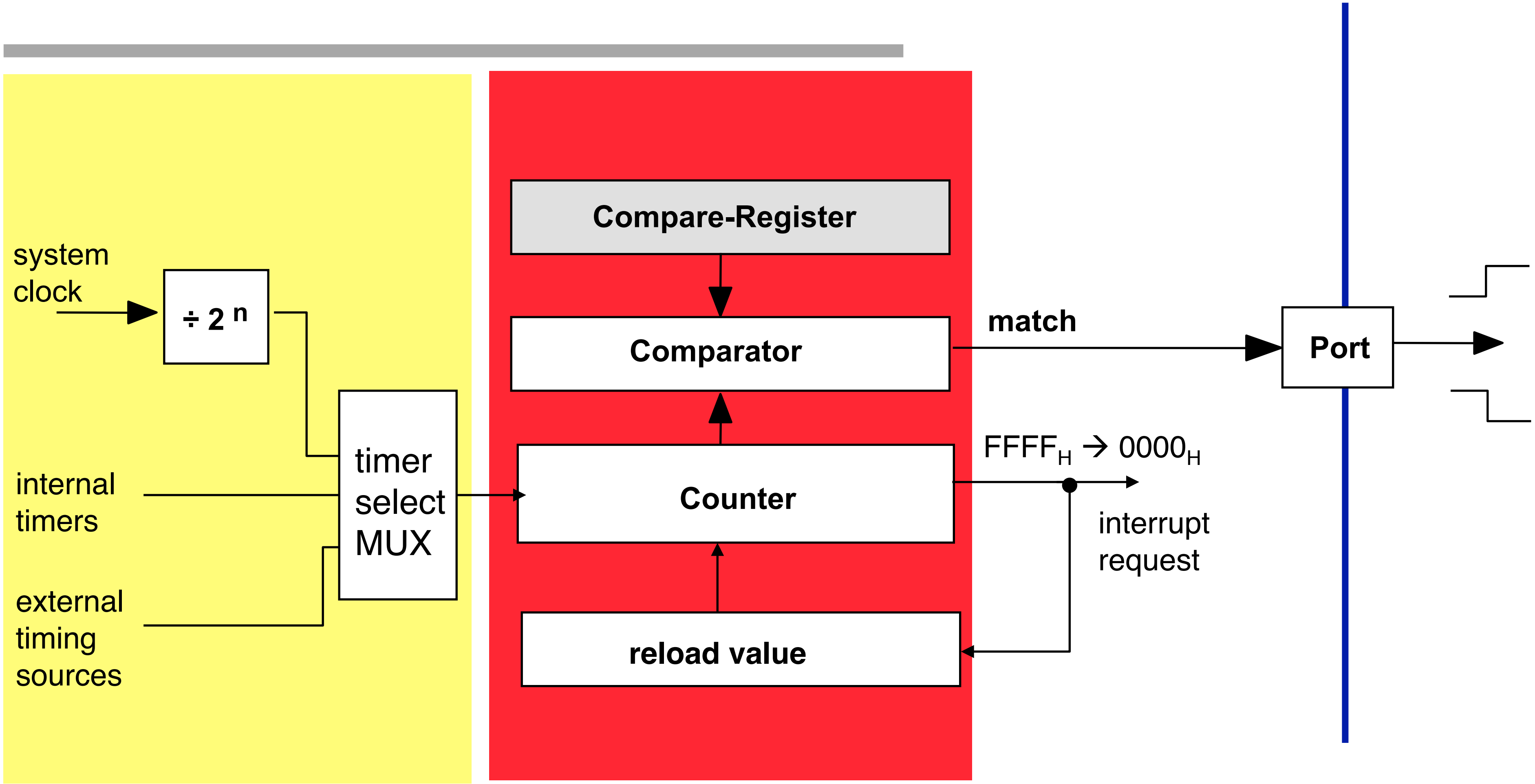
Zählermodus



Zeitgeber (Timer) -Modus

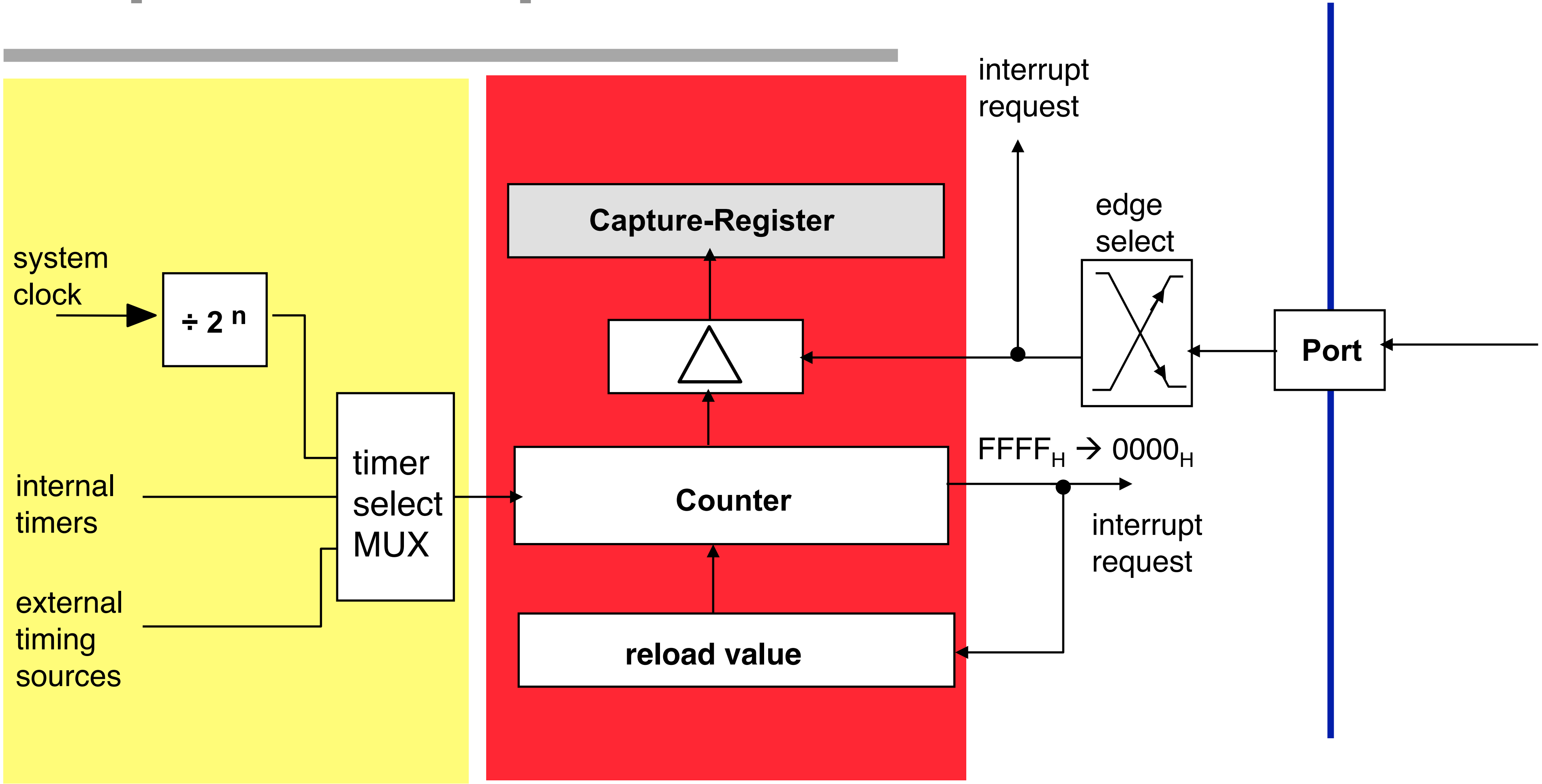


Compare Component



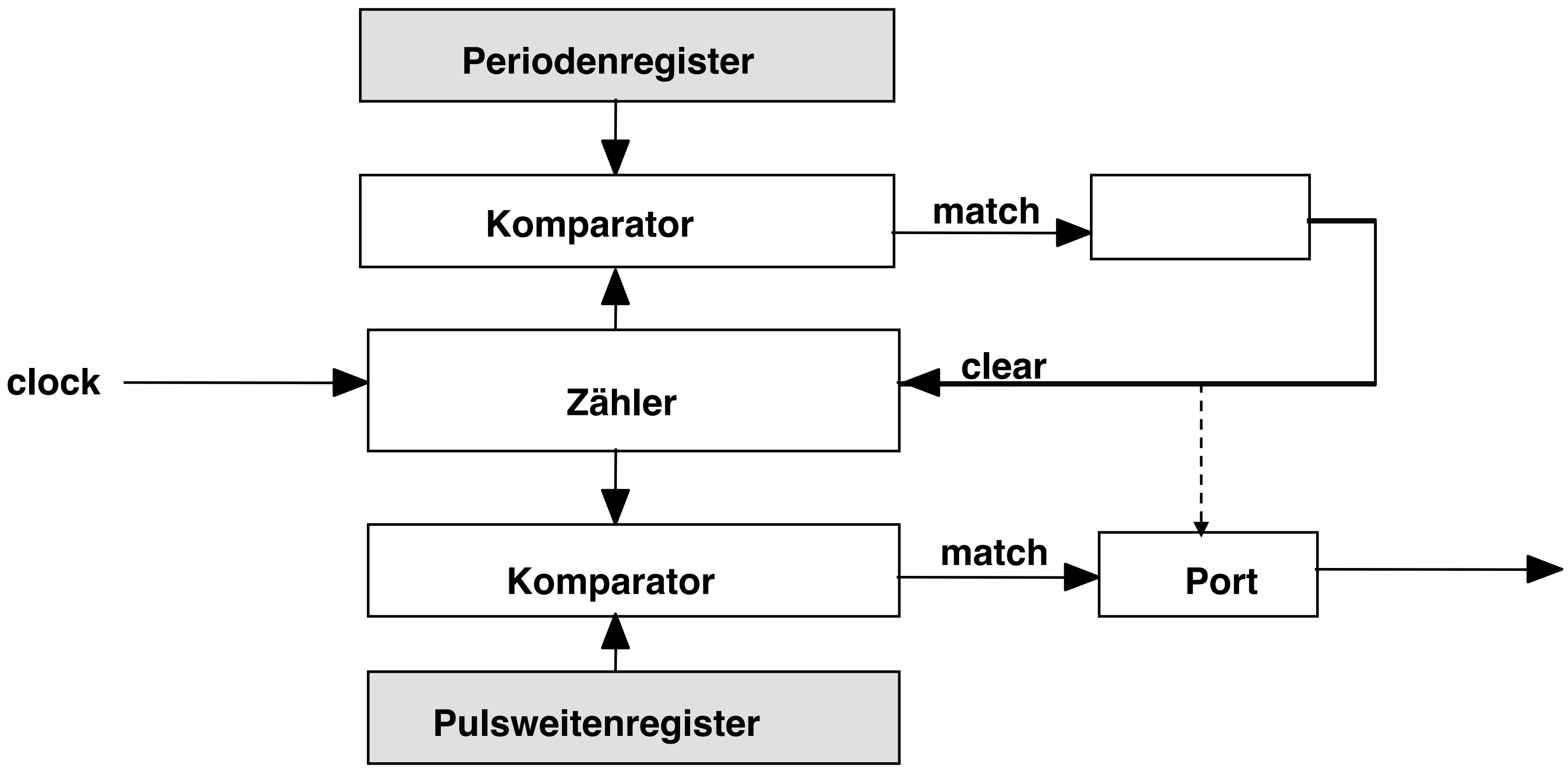
Function: Generation of time intervals
Generation of puls trains

Capture Component



Function: Generation of time stamps for external events

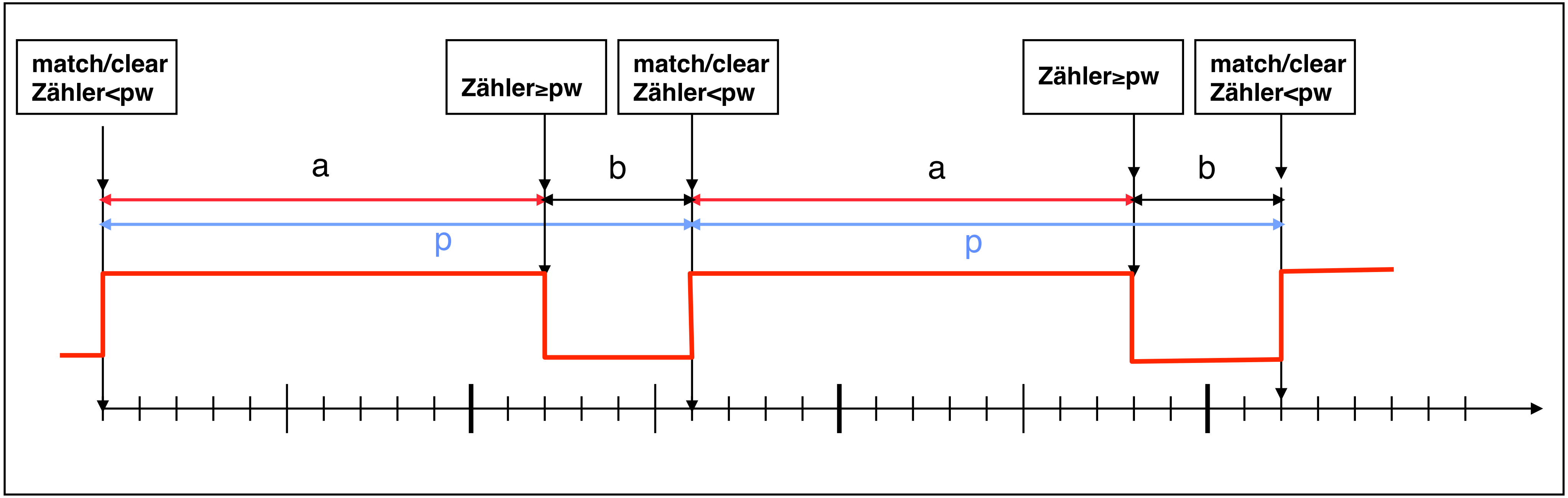
PWM (Puls-Width-Modulation) Komponente

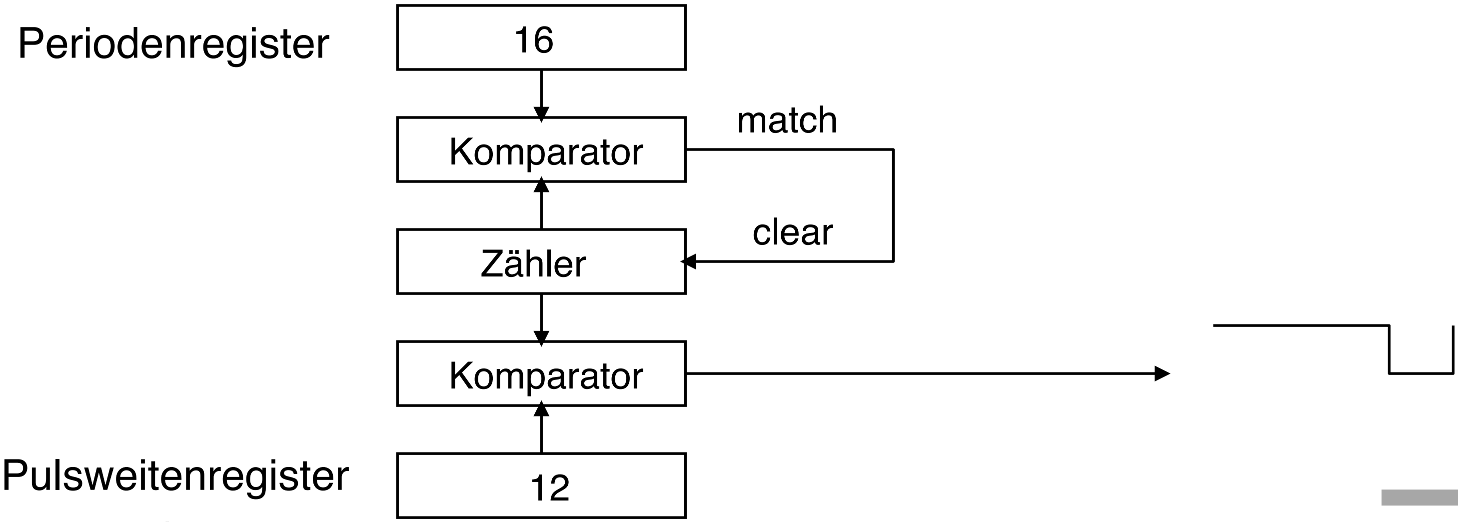


Funktion: Erzeugen von Impulsfolgen mit einer programmierbaren Frequenz und einem programmierbaren Tastverhältnis.

Beispiel: Periode p=16

Pulsweite: pw=12 Tastverhältnis: a:b = 12:4

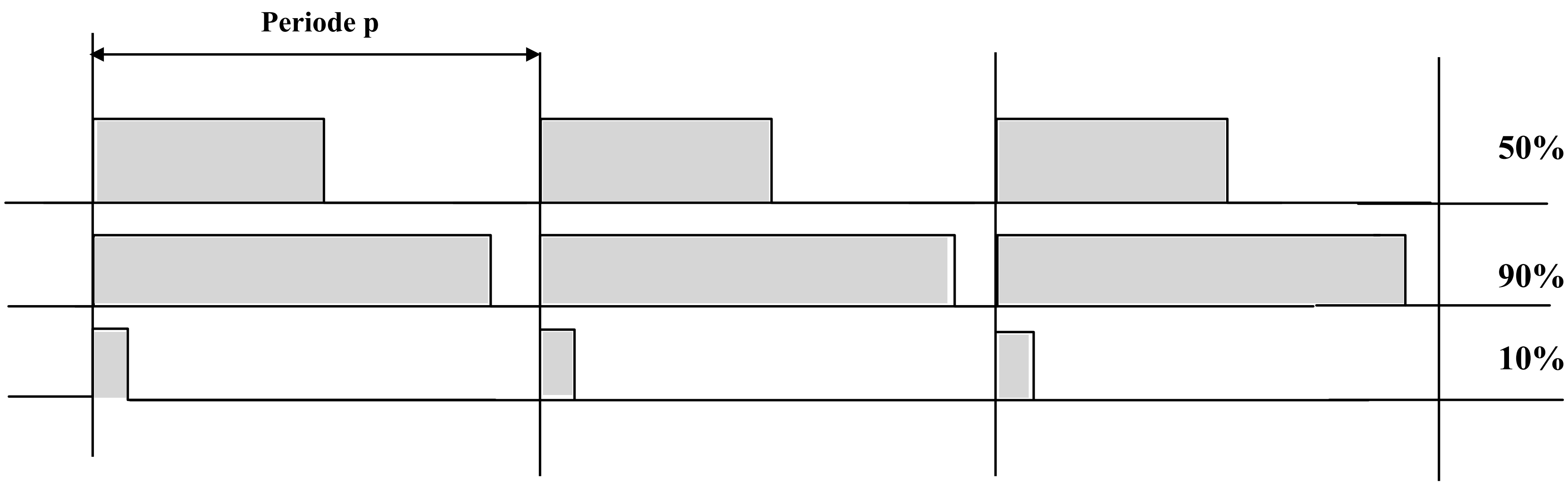




Pulsweitenmodulation

Periode und Tastverhältnis (duty cycle)

Tastverhältnis: Verhältnis des aktiven Signalpegels zum passiven Signalpegel in einer Signalperiode p.



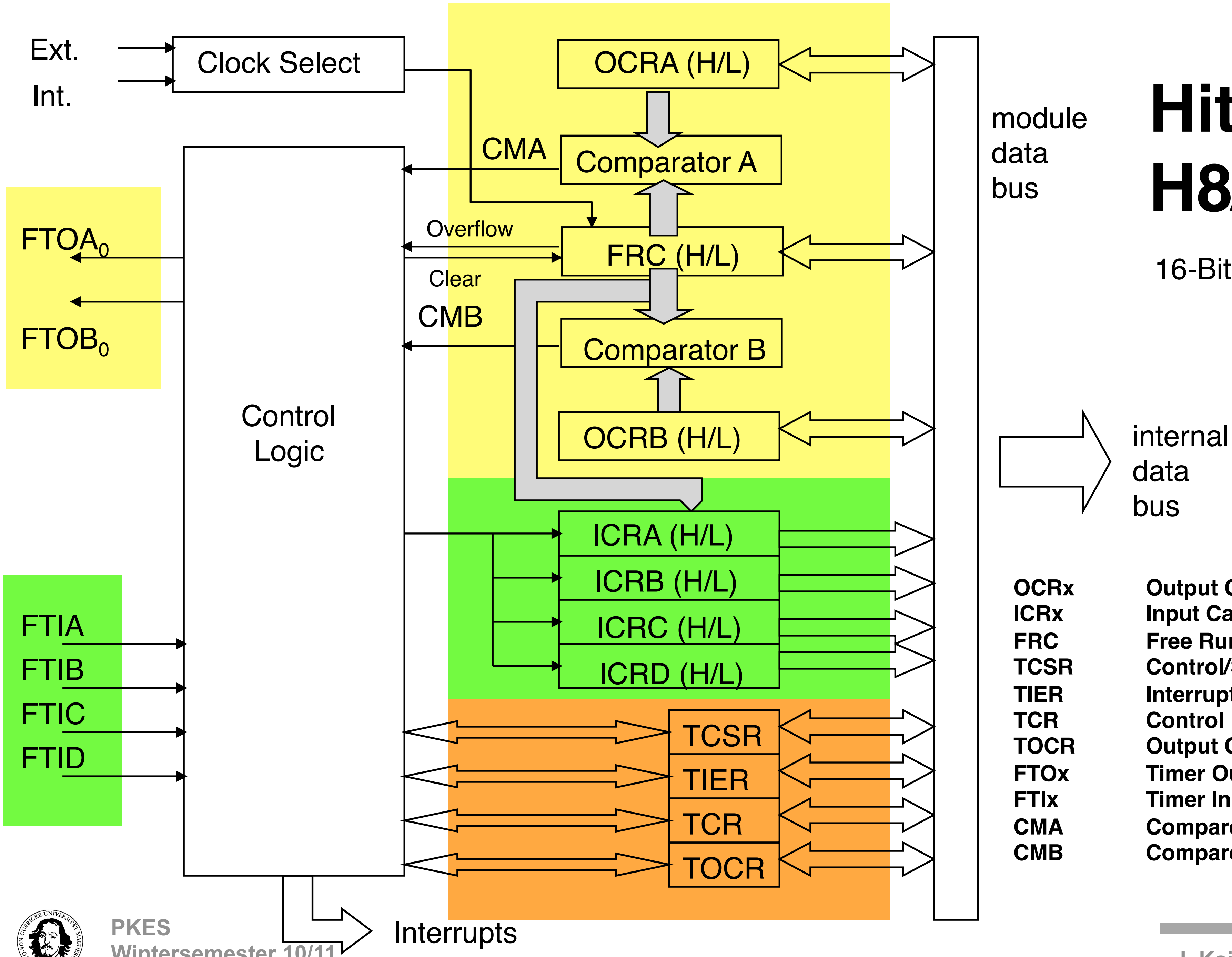
H8/300

3 x 8-Bit Zähler/Zeitgeber

1 x 16-Bit Zähler/zeitgeber (freilaufend)

Hitachi H8/300

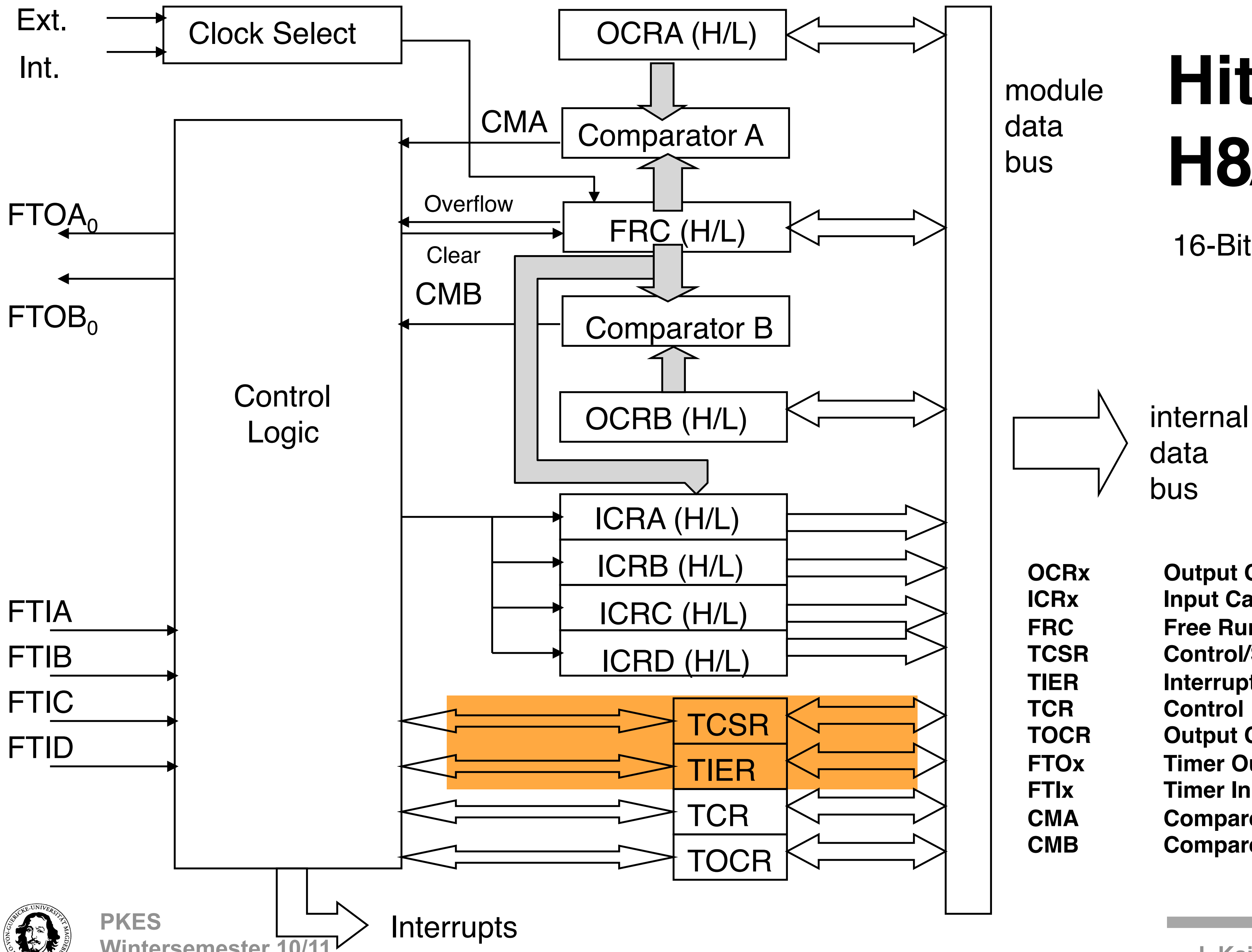
16-Bit Timer-Unit



OCRx	**Output Compare Reg.**
ICRx	**Input Capture Reg.**
FRC	**Free Running Counter**
TCSR	**Control/Status Reg.**
TIER	**Interrupt Enable Reg.**
TCR	**Control Reg.**
TOCR	**Output Compare Cntr.**
FTOx	**Timer Output**
FTIx	**Timer Input**
CMA	**Compare Match A**
CMB	**Compare Match B**

Hitachi H8/300

16-Bit Timer-Unit



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Timer Interrupt Enable Register (TIER)

Bit	7	6	5	4	3	2	1	0
	ICIAE	ICIBE	ICICE	ICIDE	OCIAE	OCIBE	OVIE	—
Initial value	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

ICIAE: Input Capture Interrupt A Enable (0: disable; 1: enable)
ICIBE, ICICE, ICIDE similar.

OCIAE: Output Compare Interrupt A Enable, Interrupt Flag for Compare/Match on OCRA
OCIAB: Output Compare Interrupt A Enable, Interrupt Flag for Compare/Match on OCRB

OVIE: Timer Overflow Interrupt Enable

Timer Control/Status Register

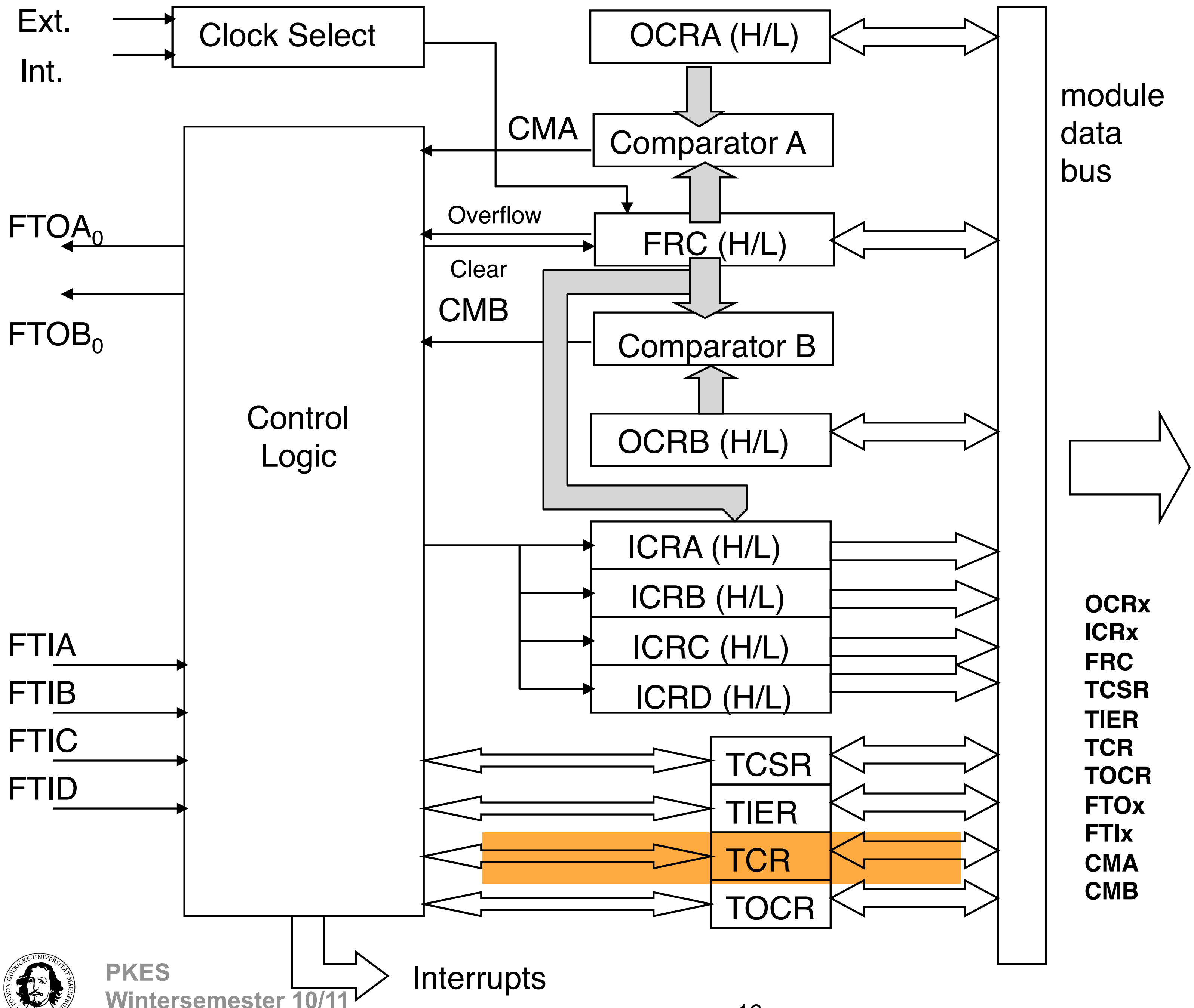
Bit	7	6	5	4	3	2	1	0
	ICFA	ICFB	ICFC	ICFD	OCFA	OCFB	OVF	OCLRA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/W

* durch Beschreiben mit "1" kann man die Flags zurücksetzen.
Ein Beschreiben mit "0" (setzen) ist nur durch das HW-Ereignis möglich.

ICF{A,B,C,D}: Input Capture Flag {A,B,C,D}, flags an input capture
OCF{A,B}: Output Compare Flag {A, B}, flags an match of FRC with OCR{A, B}.
OVF: Timer Overflow Flag
OCLRA: selects whether to clear FRC after a compare/match or not

Hitachi H8/300

16-Bit Timer-Unit



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CMB	**Compare Match B**

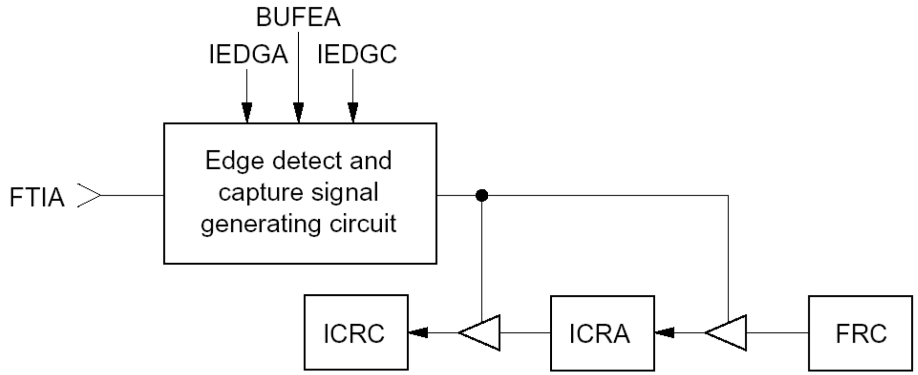
Timer Control Register

Bit	7	6	5	4	3	2	1	0
	IEDGA	IEDGB	IEDGC	IEDGD	BUFEA	BUFEB	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IEDG{A,B,C,D}: Input Edge Select {A,B,C,D}
BUFEA: Buffer Enable, selects whether to use ICRC as buffer for ICRA*
BUFEB: Buffer Enable, selects whether to use ICRD as buffer for ICRB*
Cks{0,1}: Clock select
- 00: internal clock/2
- 01: internal clock/4
- 10: internal clock/8
- 11: external clock

* If buffered mode is selected, only the inputs FTIA and FTIB are active. The control bits IEDGC and IEDGD are then used as additional bits to define the trigger levels of the inputs FTIA and FTIB respectively (see next slide).

Input Capture Control by TCR

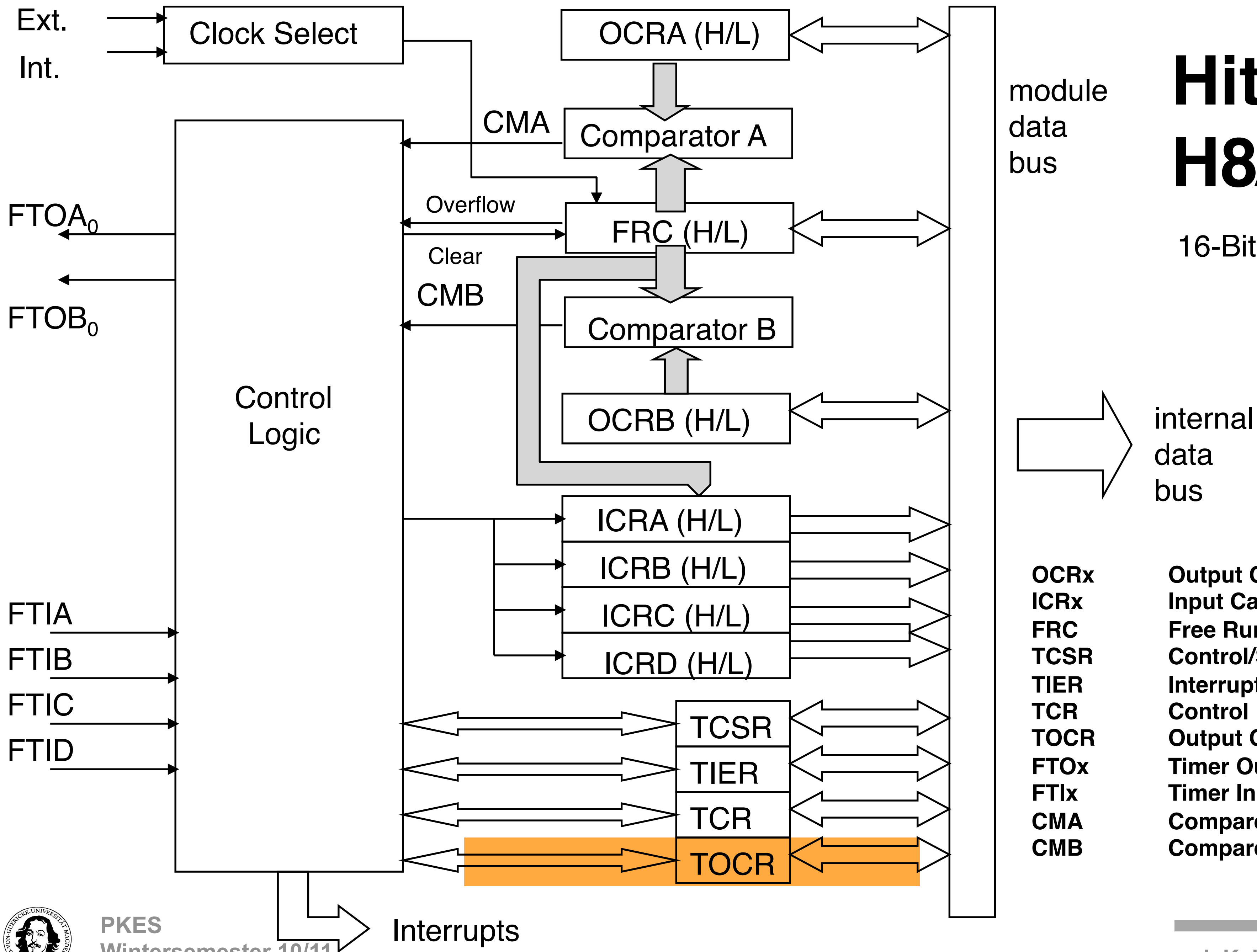


BUFEA: Buffer enable A
IEDGA: Input edge select A
IEDGC: Input edge select C
ICRC: Input capture register C
ICRA: Input capture register A
FRC: Free-running counter

IEDGA	**IEDGC**	**Input Capture Edge**
0	0	Captured on falling edge of input capture A (FTIA) (Initial value)
0	1	Captured on both rising and falling edges of input capture A (FTIA)
1	0	
1	1	Captured on rising edge of input capture A (FTIA)

Hitachi H8/300

16-Bit Timer-Unit



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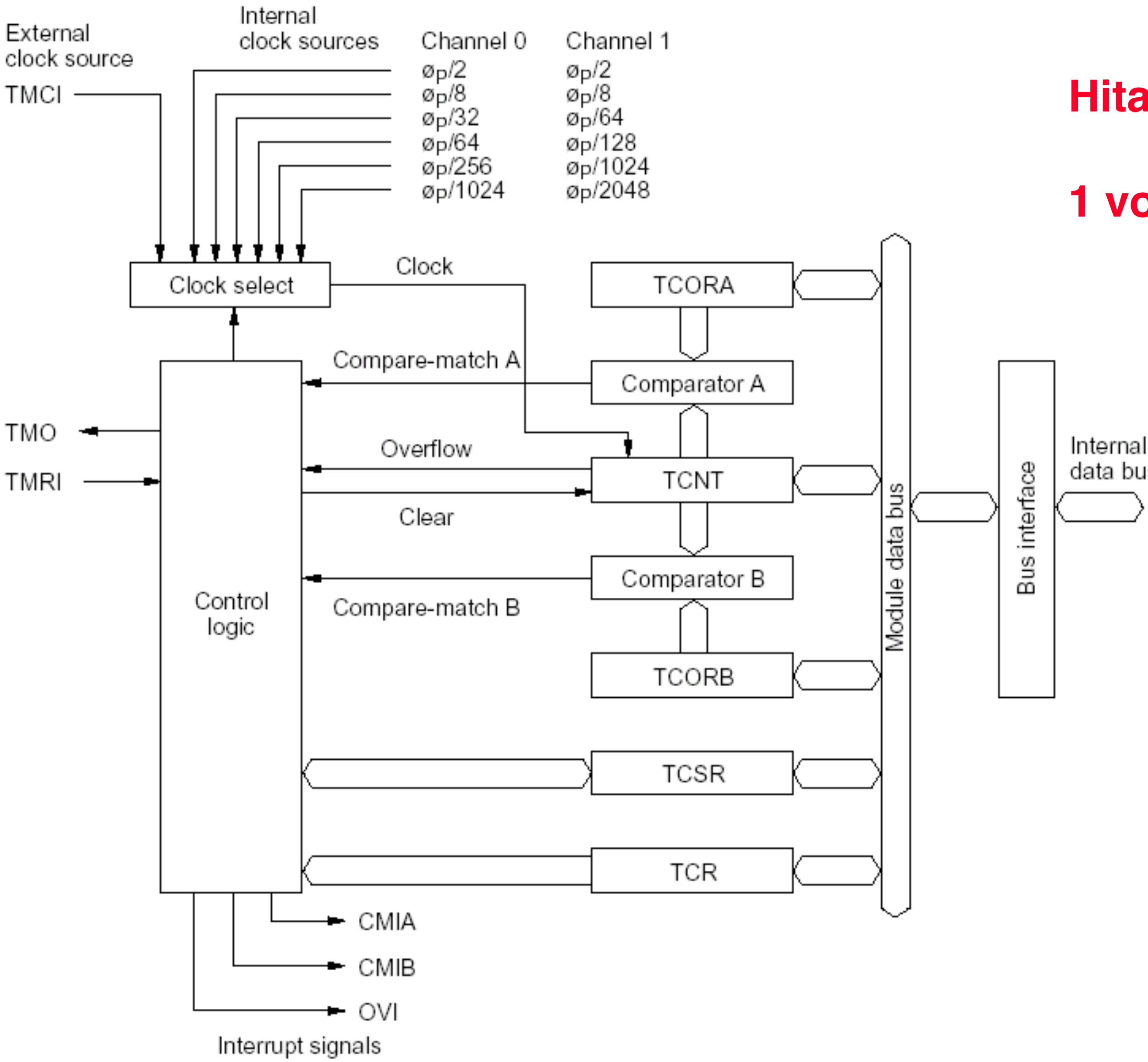
TOCR	**Output Compare Cntr.**
FTOx	**Timer Output**
FTIx	**Timer Input**
CMA	**Compare Match A**
CMB	**Compare Match B**

Timer Output Compare Control Register (TOCR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	OCRS	OEA	OEB	OLVLA	OLVLB
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

OCRS: Output Compare Register Select, OCRA and OCRB share the same address.
The OCRS defines which Register is selected.
OE{A,B}: Output Enable, enables/disables FTO{A,B}.
OVL{A,B}: Output Level, selects the logic level on FTO{A,B} when FRC and OCR{A,B} values match.



Hitachi: 8-Bit Timer

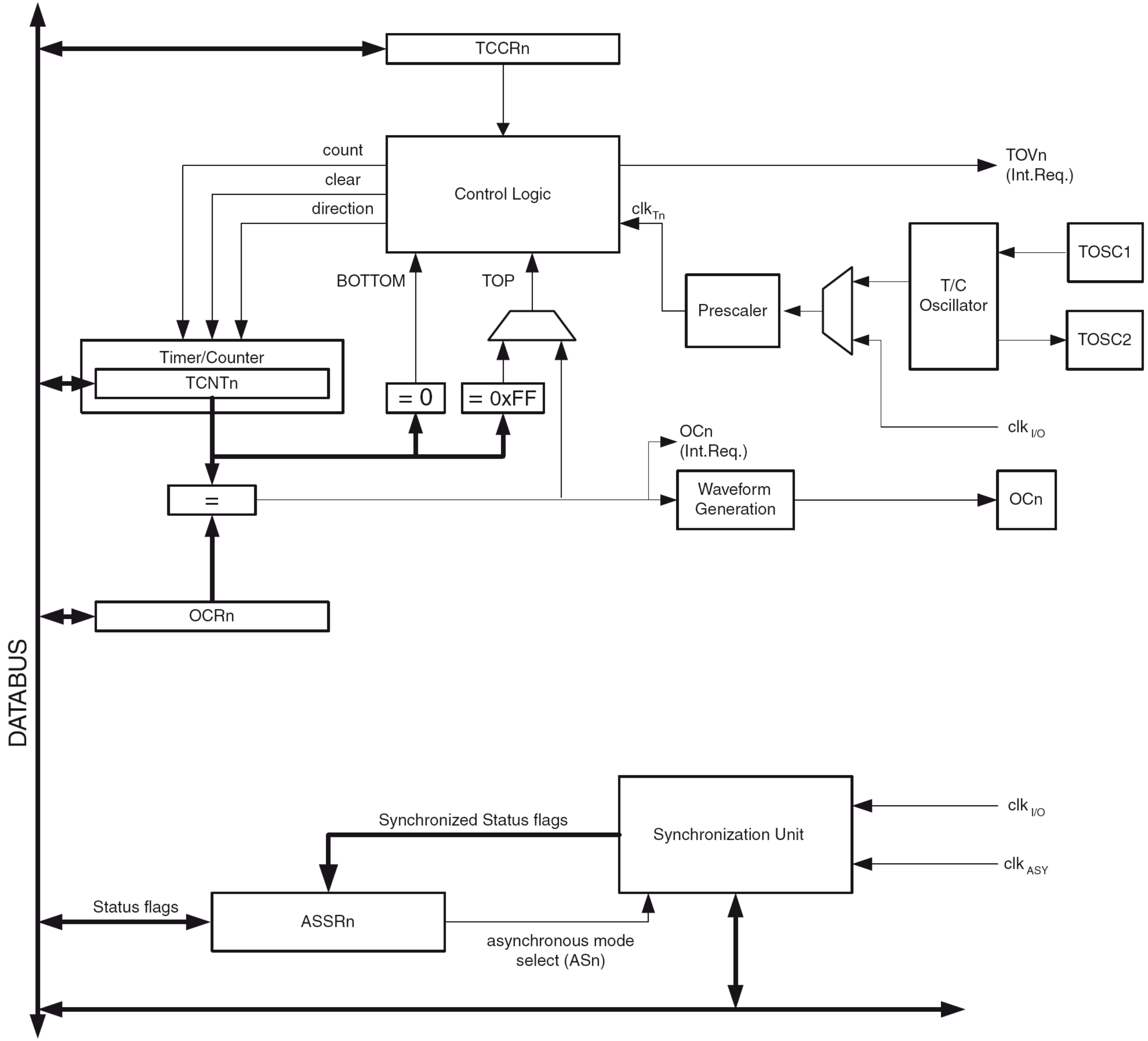
1 von 3 identischen Einheiten

TCR: Timer control register (8 bits)
TCSR: Timer control status register (8 bits)
TCORA: Time constant register A (8 bits)
TCORB: Time constant register B (8 bits)
TCNT: Timer counter

ATMEL ATmega 128

– Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
– Two Expanded 16-bit Timer/Counters with Separate Prescaler, Compare Mode and Capture Mode
– Real Time Counter with Separate Oscillator
– Two 8-bit PWM Channels
– 6 PWM Channels with Programmable Resolution from 2 to 16 Bits
– Output Compare Modulator

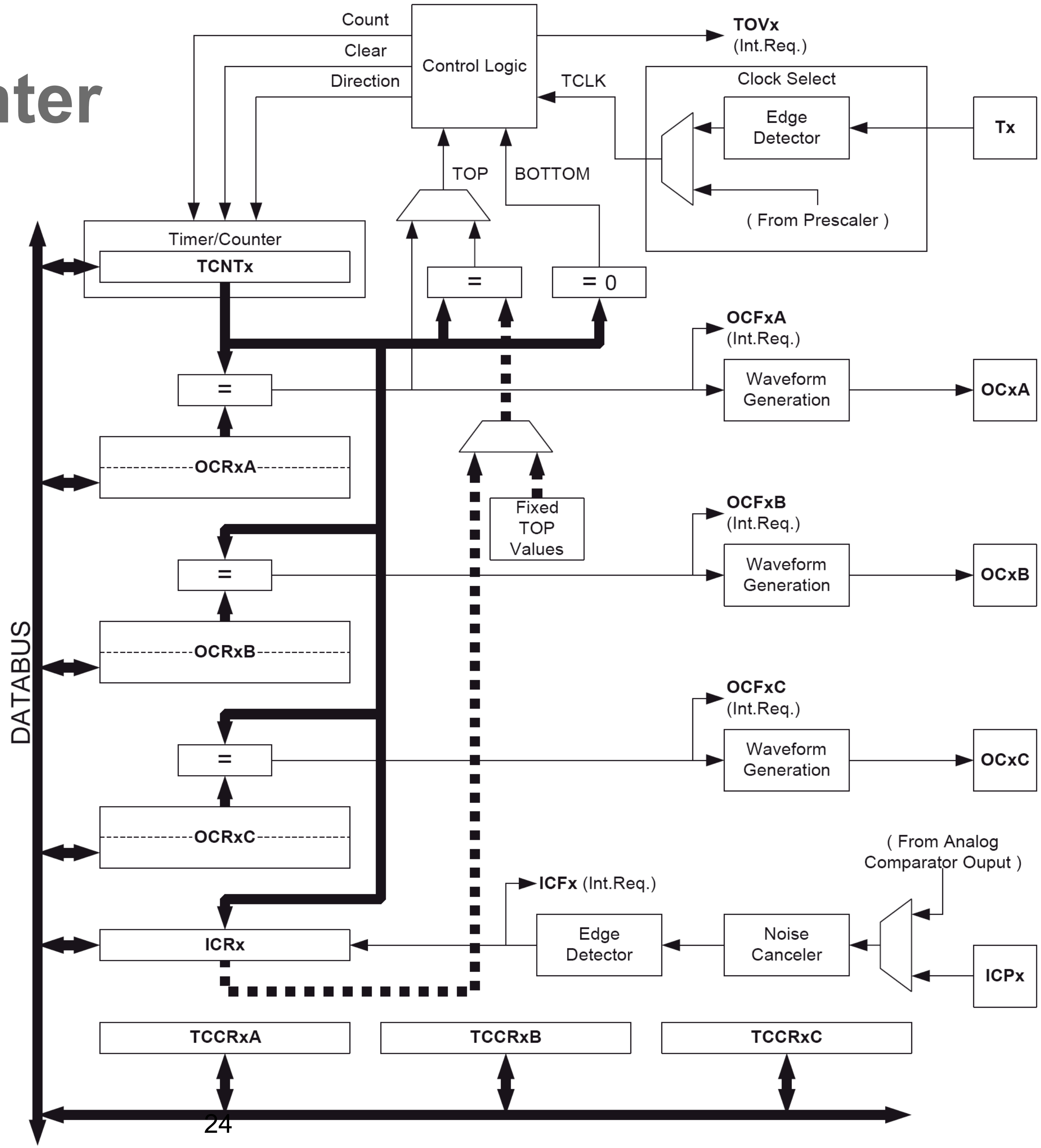
8-bit Timer/Counter0 with PWM and Asynchronous Operation



- Single Channel Counter
- Clear Timer on Compare Match (Auto Reload)
- Glitch-free, Phase Correct Pulse Width Modulator (PWM)
- Frequency Generator
- 10-bit Clock Prescaler
- Overflow and Compare Match Interrupt Sources (TOV0 and OCF0)
- Allows Clocking from External 32 kHz Watch Crystal Independent of the I/O Clock (Async. Cntr.)

16-bit Timer/Counter

- True 16-bit Design (i.e.,Allows 16-bit PWM)
- Three Independent Output Compare Units
- Double Buffered Output Compare Registers
- One Input Capture Unit
- Input Capture Noise Canceler
- Clear Timer on Compare Match (Auto Reload)
- Glitch-free, Phase Correct Pulse width Modulator (PWM)
- Variable PWM Period
- Frequency Generator
- External Event Counter



Wesentliche Punkte:

Mikro-Controller enthalten eine Vielzahl von Zeitgebern und Zählern. Die Taktraten und die Taktquellen sind flexibel wählbar.

Capture-Einheiten dienen dazu, Zeitstempel für externe und interne Ereignisse zu generieren.

Compare-Einheiten dienen dazu, Impulsfolgen mit variablen Längen, Frequenzen und Taktverhältnissen zu generieren.

PWM-Einheiten sind spezielle Compare-Einheiten die mit Perioden- und Pulsweitenregister speziell für entsprechende Steuerung externer Verbraucher ausgelegt sind.